Amendments to the Claims:

This listing of Claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Original) A silicon carbide metal-oxide semiconductor field effect transistor unit cell, comprising:

an n-type silicon carbide drift layer;

a first p-type silicon carbide region adjacent the drift layer;

a first n-type silicon carbide region within the first p-type silicon carbide region;

an oxide layer on the drift layer, the first p-type silicon carbide region, and the first n-type silicon carbide region; and

an n-type silicon carbide limiting region disposed between the drift layer and a portion of the first p-type silicon carbide region, wherein the n-type limiting region has a carrier concentration that is greater than a carrier concentration of the drift layer.

2. (Original) A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 1, wherein the portion of the first p-type silicon carbide region is adjacent a floor of the first p-type silicon carbide region.

3. (Original) A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 1, wherein the n-type limiting region is disposed adjacent a sidewall of the first p-type silicon carbide region.

4. (Original) A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 1, wherein the n-type limiting region comprises a first portion disposed adjacent a floor of the first p-type silicon carbide region and a second portion disposed adjacent a sidewall of the first p-type silicon carbide region, and wherein the first portion has a carrier concentration greater than a carrier concentration of the second portion.

5. (Original) A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 1, wherein the first p-type silicon carbide region is implanted with aluminum.

6. (Original) A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 1, further comprising:

a gate contact on the oxide layer;

a source contact on the first n-type silicon carbide region; and

a drain contact on the drift layer opposite the oxide layer.

7. (Original) A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 1, wherein the n-type limiting region comprises an epitaxial layer of silicon carbide on the n-type silicon carbide drift layer.

8. (Original) A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 7, wherein the first p-type region is disposed in but not through the epitaxial layer of silicon carbide.

9. (Original) A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 1, wherein the n-type limiting region has a thickness of from about 0.5 μm to about 1.5 μm and a carrier concentration of from about 1×10^{15} to about 5×10^{17} cm^{-3}.

10. (Original) A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 6, wherein the gate contact comprises polysilicon or metal.

11. (Original) A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 1, further comprising an n-type epitaxial layer on the first p-type silicon carbide region and a portion of the first n-type region, and disposed

between the first n-type silicon carbide region and the first p-type silicon carbide region and the oxide layer.

12. (Original) A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 1, wherein the n-type limiting region comprises an implanted n-type region in the drift layer.

13. (Original) A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 6, further comprising an n-type silicon carbide substrate disposed between the drift layer and the drain contact.

14. (Original) A silicon carbide metal-oxide semiconductor field effect transistor unit cell according to Claim 1, further comprising a second p-type silicon carbide region disposed within the first p-type silicon carbide region and adjacent the first n-type silicon carbide region.

15. (Original) A silicon carbide metal-oxide semiconductor field effect transistor, comprising:

a drift layer of n-type silicon carbide;

first regions of p-type silicon carbide adjacent the drift layer;

a first region of n-type silicon carbide disposed between peripheral edges of the first regions of p-type silicon carbide;

second regions of n-type silicon carbide within the first regions of p-type silicon carbide, wherein the second regions of n-type silicon carbide have a carrier concentration greater than a carrier concentration of the drift layer and are spaced apart from the peripheral edges of the first regions of p-type silicon carbide;

an oxide layer on the drift layer, the first region of n-type silicon carbide and the second regions of n-type silicon carbide;

third regions of n-type silicon carbide disposed beneath the first regions of p-type silicon carbide and between the first regions of p-type silicon carbide and the drift layer,

wherein the third regions of n-type silicon carbide have a carrier concentration greater than the carrier concentration of the drift layer;

source contacts on portions of the second regions of n-type silicon carbide;

a gate contact on the oxide layer; and

a drain contact on the drift layer opposite the oxide layer.

16. (Original) A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 15, wherein the third regions of n-type silicon carbide are adjacent the peripheral edges of the first regions of p-type silicon carbide.

17. (Original) A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 15, wherein the first region of n-type silicon carbide and the third regions of n-type silicon carbide comprise an n-type silicon carbide epitaxial layer on the drift layer, and wherein the first regions of p-type silicon carbide are formed in the n-type silicon carbide epitaxial layer.

18. (Original) A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 15, wherein the first region of n-type silicon carbide comprises a region of the drift layer.

19. (Original) A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 18, wherein the third regions of n-type silicon carbide comprise implanted n-type regions in the drift layer.

20. (Original) A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 15, wherein the first region of n-type silicon carbide has a higher carrier concentration than a carrier concentration of the drift layer and has a lower carrier concentration than a carrier concentration of the third regions of n-type silicon carbide.

21. (Original) A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 15, further comprising an n-type epitaxial layer of silicon carbide on the first p-type regions and the first region of n-type silicon carbide.

22. (Original) A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 15, further comprising an n-type silicon carbide layer between the drift layer and the drain contact, wherein the n-type silicon carbide layer has a higher carrier concentration than the carrier concentration of the drift layer.

23. (Original) A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 22, wherein the n-type silicon carbide layer comprises an n-type silicon carbide substrate.

24. (Original) A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 15, further comprising second p-type silicon carbide regions disposed within the first p-type silicon carbide regions.

25. (Original) A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 15, wherein the third regions of n-type silicon carbide have a thickness of from about 0.5 μm to about 1.5 μm.

26. (Original) A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 15, wherein the third regions of n-type silicon carbide have a carrier concentration of from about 1×10^{15} to about 5×10^{17} cm^{-3}.

27. (Original) A silicon carbide metal-oxide semiconductor field effect transistor comprising:

an n-type silicon carbide drift layer;

spaced apart p-type silicon carbide well regions; and

an n-type silicon carbide limiting region disposed between the well regions and the drift layer.

28. (Original) A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 27, wherein the n-type limiting region is disposed between the spaced apart p-type well regions.

29. (Original) A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 27, wherein the n-type limiting region has a carrier concentration higher than a carrier concentration of the drift layer.

30. (Original) A silicon carbide metal-oxide semiconductor field effect transistor according to Claim 27, wherein the n-type limiting region comprises an epitaxial layer of silicon carbide on the drift layer, and wherein the p-type well regions are disposed in but not through the epitaxial layer.

31. – 60. (Canceled.)